REMARKS

35 U.S.C. § 103 Rejections

The Examiner has rejected claims 1-12, 16, 29, 30 and 32 under 35 U.S.C. §103(a) as being unpatentable over Rodder in view of Sekine and Ishida.

Claim 1 includes reacting the metal layer with the semiconductor material of the substrate to form two silicide regions having upper portions of inner surfaces thereof that contact the alignment component and removing the alignment component. Specifically, claim 1 includes the limitations "reacting the metal layer with the semiconductor material of the substrate to form two silicide regions, the silicide regions having inner surfaces which face one another, wherein an upper portion of each inner surface contacts the alignment component," and "removing the alignment component."

Rodder does not teach or suggest reacting the metal layer with the semiconductor material of the substrate to form two silicide regions having upper portions of inner surfaces thereof that contact the alignment component and removing the alignment component. Rodder teaches a method for forming a MOSFET transistor 100 using a disposable gate 120 (Abstract). As shown in Figure 3A, a disposable gate 120 is formed on an active area of substrate 102 over the region where the channel region of MOSFET 100 is desired (Column 2, lines 59-64). Next, raised source-drain regions 106 are formed (Column 3, line 5). The raised source-drain regions 106 are then doped with an appropriate dopant (Column 3, lines 21-22). As clearly shown in Figures 3A - 3D, the upper portions of the inner surfaces of

the source and drain regions 106 do not contact the alignment component. Rodder thus teaches forming silicide regions on a substrate without the silicide regions contacting the alignment component. Specifically, Rodder does not teach or suggest reacting the metal layer with the semiconductor material of the substrate to form two silicide regions having upper portions of inner surfaces thereof that contact the alignment component and removing the alignment component.

Sekine does not teach or suggest reacting the metal layer with the semiconductor material of the substrate to form two silicide regions having upper portions of inner surfaces thereof that contact the alignment component and removing the alignment component. Sekine teaches fabrication steps of a MOS transistor for forming a sidewall corresponding to a sidewall forming method and for forming corresponding to an application of a silicide technique (Column 7, lines 40-44). A field oxide film 103 is formed on a P-type or N-type semiconductor substrate 101 (Column 7, lines 46-47). Then a gate oxide film 104 is formed in a transistor-forming region surrounded by the field oxide film 103 (Column 7, lines 47-51). Next, an amorphous silicon or polysilicon film 105 and a Phospho-Silicate Glass (PSG) film 107 are successively formed on the entire surface of the substrate 101 (Column 7, lines 51-56). After etching, the polysilicon film 105 and the PSG film 107 which remain become members of the gate electrode (Column 7, lines 64-65). After that, a silicon nitride film 110 is formed on the entire front surface of the substrate to form a sidewall of the gate electrode (Column 7, line 66 – Column 8, line 3). After the fabrication steps as shown in Figures 1A – 1D, an ion implantation

process in a heat treatment are performed for the polysilicon film to form source and drain regions 111 (Column 8, lines 27-38). As clearly illustrated in Figures 2A - 2D, the source and drain regions to not contact any alignment component. Sekine thus teaches forming source and drain regions within a substrate that do not contact any alignment component. Specifically, Sekine does not teach or suggest reacting the metal layer with the semiconductor material of the substrate to form two silicide regions having upper portions of inner surfaces thereof that contact the alignment component and removing the alignment component.

Ishida does not teach or suggest reacting the metal layer with the semiconductor material of the substrate to form two silicide regions having upper portions of inner surfaces thereof that contact the alignment component and removing the alignment component. Ishida teaches a process of manufacturing raised source-drain MOSFETs (Abstract). As shown in Figure 4A, a layer of doped amorphous silicon 550 is deposited or otherwise formed over substrate 510 (Column 4, line 67 - Column 5, line 2). The amorphous silicon can be doped by ion implantation or by other doping methods (Column 5, lines 2-4). As shown in Figure 4C, once the doped amorphous silicon layer 550 has been formed on a substrate 510, layer 550 is patterned and etched to form window 590 (Column 5, lines 32-34). Using high temperatures, dopants are driven from the doped amorphous silicon 550 into the substrate 510 to form shallow source and drain regions 540 (Column 5, lines 64-67). As clearly shown in Figures 4D and 4E, the source and drain regions 540 do not contact the window 590. Ishida thus teaches forming shallow source and drain

regions within a substrate which do not contact any alignment component. Specifically, Ishida does not teach or suggest reacting the metal layer with the semiconductor material of the substrate to form two silicide regions having upper portions of inner surfaces thereof that contact the alignment component and removing the alignment component.

Therefore, claim 1 is patentable over Rodder in view of Sekine and Ishida because claim 1 includes limitations that are not taught or suggested in Rodder, Sekine, and Ishida.

Claims 2-12, 16, 29, 30, and 32 are dependent on claim 1 and should be allowable for the same reasons above.

Applicant, accordingly, respectfully requests withdrawal of the rejection of claims 1-12, 16, 29, 30 and 32 under 35 U.S.C. § 103(a) as being unpatentable over Rodder in view of Sekine and Ishida.

The Examiner has rejected claims 13-15 and 31 under 35 U.S.C. § 103(a) as being unpatentable over Rodder in view of Sekine and Ishida and further in view of Inumiya.

Claims 13-15 and 31 are dependent on claim 1 and should be allowable for the same reasons above.

Applicant, accordingly, respectfully requests withdrawal of the rejection of claims 13-15 and 31 under 35 U.S.C. § 103(a) as being unpatentable over Rodder in view of Sekine and Ishida and further in view of Inumiya.

The Examiner has rejected claims 17-19 under 35 U.S.C. § 103(a) as being unpatentable over Rodder, Sekine, Ishida, and Inumiya as applied to claims 1 and 13 above, and further in view of Gardner.

Claims 17-19 are dependent on claim 1 and should be allowable for the same reasons above.

Applicant, accordingly, respectfully requests withdrawal of the rejection of claims 17-19 under 35 U.S.C. § 103(a) as being unpatentable over Rodder, Sekine, Ishida, and Inumiya, and further in view of Gardner.

The Examiner has rejected claim 28 under 35 U.S.C. § 103(a) as being unpatentable over Rodder, Sekine and Ishida, as applied to claims 1 above, and further in view of Wolf.

Claim 28 is dependent on claim 1 and should be allowable for the same reasons above.

Applicant, accordingly, respectfully requests withdrawal of the rejection of claim 28 under 35 U.S.C. § 103(a) as being unpatentable over Rodder, Sekine and Ishida, and further in view of Wolf.

Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist

in the allowance of the present application, the Examiner is invited to call Michael A. Bernadicou at (408) 720-8300.

Please charge any shortages and credit any overages to Deposit Account No. 02-2666. Any necessary extension of time for response not already requested is hereby requested. Please charge any corresponding fee to Deposit Account No. 02-2666.

Respectfully submitted,

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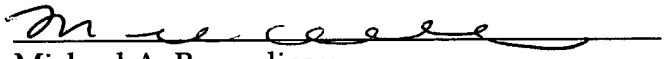

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